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Detailed analysis and understanding of the transport mechanism of poly-Si based carrier selective junctions

Andrej Čampa, Franc Smole, Nils Folchert, Tobias Wietler, Byungsul Min, Rolf Brendel, and Marko Topič

Abstract— We investigate the transport mechanism of poly-Si based carrier-selective junctions using the 2-D numerical semiconductor device simulations. The detailed transport model considers the charge carrier transport through the pinholes as well as tunnelling through a very thin silicon oxide simultaneously. For the verification of the simulation model, the complete temperature dependent transfer length method was modelled and its results were verified with measurements of two different samples. By means of rigorous simulations, the influence of different pinhole geometrical and material parameters on junction resistivity was investigated and explained in detail. From the presented results the fundamental understanding needed for optimizing the poly-Si based carrier selective junction in respect to the main design parameters such as doping level in poly-Si, annealing time, silicon oxide thickness and pinhole density is given. The detailed analysis showed the pinhole channel plays the most crucial role in the design of poly-Si based carrier-selective junctions if the silicon oxide layer thickness is larger than 2 nm.

Index Terms—carrier-selective junctions, numerical simulations, polysilicon on oxide, pinholes, tunneling.

I. INTRODUCTION

IN the recent years the silicon wafer photovoltaics (PV) technology has matured in the extents the minority carrier lifetimes in the state-of-the-art low doped silicon wafers are relatively high ($\tau_{e,h} > 1$ ms). Therefore the main limiting efficiency factor in the high efficiency Si solar cells has shifted mainly to the support layers and their electric and optical losses, particularly their interface electrical losses. For highly efficient solar cells the efficient carrier selective separation mechanism is of great importance [1],[2]. Therefore various carrier-selective junctions that simultaneously also efficiently

passivate contacts are becoming of great interest [3]. In the amorphous silicon-based heterojunction solar cells (HJT) carrier-selective junction is already a well-established technology [4],[5]. Recently the research has been focusing on new carrier-selective junctions based on the various materials such as MoOx [6], TiOx[7],[8], WOx [9] and VOx[10]. In this work, we have focused on well known and established polycrystalline silicon (poly-Si) based carrier-selective junctions (CSJ) that had been the main topic in bipolar transistors [11],[12] and are becoming important also in the field of PV under the names POLO or TOPCon. The main advantages of the poly-Si based CSJs are (i) the technology is already well established, (ii) they exhibit excellent interface passivation properties thanks to a very thin SiO_x interface layer. Through the very thin SiO₂ interface layer transport of carriers by means of tunnelling [13],[14], by means of pinholes [15],[16] or by a combination of both mechanisms [17] is considered. While its working principle including the current transport with pinholes is described analytically [15] as well as numerically [16], a detailed theoretical study about the influence of the material and geometrical parameters on the carrier transport is still missing. The recently achieved record cell based on CSJs achieved 26.1% energy conversion efficiency (for the interdigitated back contacted POLO Si solar cell) [18] demonstrates the importance and effectiveness of CSJ based solar cells. To exploit the ultimate potential of the poly-Si based CSJs and to understand the principal transport mechanism and other limiting parameters of CSJ based solar cells is therefore of great importance. In this work, we performed an extensive analysis of poly-Si based CSJs by rigorous 2-D models based on the drift-diffusion model. The SENTAURUS TCAD was

Manuscript received July 12, 2019 revised September 4, 2019; accepted September 20, 2019. This work was supported in part by the European Union's Horizon 2020 research and innovation programme under Grant 727529 and in part by the Slovenian Research Agency under the P2-0197 program. (Corresponding author: Andrej Čampa.)

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Digital Object Identifier 10.1109/JPHOTOV.2019.2943610

used for modelling CSJs and transfer length method (TLM) [19] was implemented in the model so the simulation results could directly be compared to the experiment [20]. The primary derived output parameter under investigation that was used as a figure of merit in the investigation was the junction resistivity (also contact resistivity) [16],[21],[22].

In this work we first present the detailed realistic 3-D structure of poly-Si based CSJ that is transformed into a 2-D equivalent structure for use in SENTAURUS TCAD, since high density ($10^6 - 10^8 \text{ cm}^{-2}$) and different scale length between pinholes size (nm range) and TLM size (range up to 1 mm) in 3-D would produce an irrational huge numeric problem to solve. After detailed verification of the model, the sensitivity analysis of vital parameters on the junction resistivity has been performed. All the detailed explanations of the obtained trends are given from semiconductor physics point of view from which the guidelines for further improvement of poly-Si based CSJs are given.

II. MODELLING AND SIMULATIONS

To analyse the poly-Si based CSJs, the proper physical and precise geometrical modelling is essential to understand and investigate the main physical parameters that influence the junction resistivity (ρ_c) [15]. Furthermore, it is crucial the structure is prepared in the way it does not use additional support layers or at least their resistances can be neglected compared to the junction resistivity under investigation. The model we chose is based on TLM test structures of CSJs [23] as shown in Fig. 1. To neglect the effect of the thick substrate layer on the TLM structure only 100 nm thin layer of the c-Si layer between contacts was considered. The doping level for the c-Si layer was 10^{17} cm^{-3} for acceptors (N_A) or donors (N_D), for p- or n-type poly-Si based CSJs, respectively. Furthermore, the width of TLM contacts (W) was set to 100 μm similar to experiment; spacing between contacts (D) was 100 μm and 200 μm for simulations and up to 1 mm with a step size of 100 μm in case of the experiment. The current applied to the contacts was set to 10 mA both in experiment and simulations. The typical pinhole radius used in simulations was 2 nm with an area density of 10^8 cm^{-2} , if not otherwise specified. Below the contact 30 nm of heavily doped (n- or p-type) poly-Si layer is considered. The default SiO_2 thickness and therefore also the length of a pinhole through the SiO_2 layer was 2 nm. The diffusion of dopants during the annealing process from the poly-Si layer into the c-Si layer was considered in simulations. In the pinholes the same material parameters of poly-Si were considered with the same doping concentration. The measured doping profiles, Fig. 7, obtained from the electrochemical

Fig. 1. Schematic presentation of the TLM structure considered in experiment and simulations.

current voltage (ECV) measurements of test structures were implemented and different doping profiles were analysed. By default, simple exponential decay fitted to measurements of diffused dopants was considered in a c-Si layer just below the SiO_2 layer. After just a few nanometres, it drops to the default doping value of c-Si.

The pinholes radius (r_p) is set to 2 nm, and pinhole area density is very high $\sim 10^8 \text{ cm}^{-2}$ which would results in $3 \cdot 10^5$ pinholes under one contact that have to be taken into consideration. Therefore we decided to reduce the 3-D problem to a 2-D equivalent one, without sacrificing the main topological features of the pinholes that might influence the junction resistivity.

A. Transformation of the 3-D problem to the 2-D equivalent problem

As we have seen the dimensions range are of few orders of magnitude since the TLM structure is in mm range and the pinholes are in nm range. Even meshing of such structure in 3-D is out of scope and furthermore solving such a nonlinear problem might become a real challenge to solve and to do any kind of analysis on this kind of structure. Therefore, we have decided to transform the 3-D structure under investigation into manageable approximation in 2-D. As shown in Fig. 2 the 3-D pinhole structure can be transformed into the 2-D structure by taking the following rules:

- Instead of a realistic random distribution of pinholes the periodic distribution of pinholes is assumed in x- and z-direction.
- The distance (L) between two pinholes is calculated by preserving the pinhole density and calculating its average distance in x and z-direction, $L = \sqrt{\frac{1}{\text{pinhole_density}}}$. In the case of pinhole areal density of 10^8 cm^{-2} , $L = 1 \mu\text{m}$.
- The cylindrical approximation of 3-D pinhole is transformed in a line pinhole in 2-D through SiO_x layer. Preserving the length of pinhole defined by the SiO_x thickness.
- The width of the 2-D transformed pinhole (line) is calculated by assuming the density of pinhole area should not change from 3-D transformation to 2-D transformation, thus keeping current densities inside the 2-D pinhole same as in the case of a realistic pinhole in 3-D. The 3-D pinhole was transformed to 2-D by preserving the current crowding in pinhole of

Fig. 2. The schematic of transforming 3-D pinholes with different areal densities to its equivalent 2-D representation.

the 3-D model. The following equation gives the width of 2-D pinhole $W_p = \frac{\pi r_p^2}{L}$ as a function of period and pinhole radius.

B. Material properties

Since typical junction resistances of poly-Si based CSJs are quite low, accurate material parameters and junction description are of great importance to make a reliable sensitivity analysis. For differently doped c-Si substrates the well-established models and parameters were used [24], such as Klaassen's mobility model [25], thermionic emission with Fermi statistic, Schenk's bandgap narrowing model [26], Intrinsic carrier density $n_i = 9.65 \times 10^9 \text{ cm}^{-3}$ [27] and Auger recombination with Richter parametrization [28]. In the case of poly-Si, SiO_2 and the two SiO_2 interfaces the most important parameters are summarised in Table 1.

TABLE I
SIMULATION PARAMETERS AND THEIR TYPICAL VALUES FOR POLY-Si, SiO_2
AND $\text{SiO}_2/\text{c-Si}$ AND $\text{SiO}_2/\text{POLY-Si}$ INTERFACES

Poly-Si [29]	
Band gap E_g	1.16 eV
Affinity X	4.05 eV
Permittivity ϵ	11.7
Electron mobility μ_e	40 cm^2/Vs
Hole mobility μ_h	5 cm^2/Vs
SRH τ_e and τ_h	50 ps
Thickness	30 nm
SiO_2	
Band gap E_g	9 eV [30]
Affinity X	0.9 eV [31]
Permittivity ϵ	3.9
Conduction band tunnelling mass	0.3 m_0 [32]
Valence band tunnelling mass	0.3 m_0 [32]
Tunnelling probability	WKB approximation [29]
Thickness	2 nm
Pinhole density	10^8 cm^{-2}
$\text{SiO}_2/\text{c-Si}$ and $\text{SiO}_2/\text{poly-Si}$ interface	
Surface recombination velocity for electrons S_{n0}	100 cm/s
Surface recombination velocity for holes S_{p0}	100 cm/s
Fixed oxide charge Q_f	$1 \sim 30 \cdot 10^{11} \text{ cm}^{-2}$ [33],[34]
ECV profiles	Fig. 7

Since the TLM method is executed in the dark (without illumination), the surface recombination velocity parameter does not play a significant role, due to the very low minority carrier density. Furthermore, simulations show (not shown here) the fixed charge (Q_f) attributed to SiO_2 interface does not influence the junction resistance. Moreover, the simulations show the tunnelling is negligible for the SiO_2 thickness of 2 nm or above, therefore if not implicitly specified, the tunnelling was neglected to speed up the numerically demanding simulations.

C. Verification of the model

By setting up the introduced TLM model in the SENTAURUS TCAD environment and with the parameters given in Table 1 we have performed the verifications of the model and compared the simulated results with measured data and to the typical

values obtained in the literature as shown in Ref. [20]. These typical values also depend on other parameters such a doping levels and pinhole geometrical properties, therefore their trends are of interest. The model was first verified on the pinhole sample followed by the tunnelling sample as described in the details in Ref. [17]. To be more consistent with the measured values from Ref. [17] we have adjusted our parameters to their calibrated values such as a radius of the pinhole (from 2 nm to 2.8 nm) and tunnelling masses to $0.23 \cdot m_0$ instead of $0.3 \cdot m_0$. This adjustment would not drastically change the results and trends presented in this work. In the case of pinhole sample, an n-type wafer was used with a resistivity of $2.3 \Omega\text{cm}$. On top of the wafer is 2.1 nm thick thermal oxide followed by 80 nm heavily doped phosphorus implanted poly-Si layer. Measured phosphorous density in the poly-Si layer was $2 \cdot 10^{20} \text{ cm}^{-3}$. During the annealing process, the dopants diffuse to the silicon layer [21]. Therefore, in the simulation a doping profile was implemented in the c-Si layer below the SiO_2 layer, an exponential decay fitted to measured values (see section 3. Results, Fig. 8). Furthermore, the pinhole density of $6.6 \cdot 10^6 \text{ cm}^{-2}$ was used in modelling as reported for this sample in Ref. [35]

Fig. 3. Junction resistance of poly-Si based CSJ as a function of temperature for (a) an n-type pinhole sample and (b) for p-type tunnelling sample with a SiO_2 thickness of 1.7 nm. The solid green lines are the calculated values and black symbols measured values from Ref. [17].

and the over-etching was implemented between contacts to remove the n-diffused region [36]. The resistance as the function of D was calculated from the presented numerical TLM model. These resistances were used with corrected TLM method [19] to obtain the corresponding contact resistivity. First, we have tested the pinhole model and its capability to describe the pinhole current. The very good agreement is obtained between measured values and simulated values for junction resistance as a function of the temperature, Figure 3 (a). These values are also quite similar to the values obtained by different authors as summarised in Ref. [17], [33]. Next, we have tested the model for tunnelling currents (Fig. 3b) through the SiO_2 layer for p-type CSJ tunnelling sample. In this case, according to the literature (Ref. [17]) the tunnelling parameters were set to $m_{e,h} = 0.23 m_0$ and energy shift was added to the valence band in WKB tunnelling to 215 meV and SiO_2 thickness of 1.7 nm was used. Those values are chosen according to the literature [17] to obtain a good match to the experiment. Again, good agreement is obtained between our simulation results of ρ_c as a function of temperature, Fig. 3 (b), confirming the validity of the used models and methods.

Fig. 4. Simulated junction resistivity as a function of temperature and poly-Si doping level for n-type (a) and p-type (b) poly-Si based CSJ obtained from TLM model.

Fig. 5. Simulated junction resistivity as a function of temperature and pinhole density for n-type (a) and p-type (b) poly-Si based CSJ obtained from TLM model.

III. RESULTS AND DISCUSSION

An extensive sensitivity analysis was done to understand the poly-Si based CSJs. In the first temperature dependent TLM analysis, we have simulated different doping levels of the poly-Si layer at a constant pinhole density of 10^8 cm^{-2} . In Fig. 4 the junction resistivity for different doping levels as a function of temperature is shown. The ρ_c decreases with increasing doping level. Furthermore, the ρ_c increases with temperature for most cases. This is especially evident for low doping levels of poly-Si. Which means the resistivity of the pinhole channel mostly defines the ρ_c . The ρ_c calculated by TLM method is a combination of true junction resistivity related to the conduction or valence band offset and pinhole channel resistivity. In the case of highly doped layers, the pinhole channel resistivity becomes smaller than resistivity associated with the band offset at the poly-Si/c-Si junction. In this case, the higher thermal energy helps charge carriers to more easily overcome the band offset, which results in the overall decrease of ρ_c with temperature. In the case of n-type poly-Si based CSJ doping levels should be higher than 10^{20} cm^{-3} to turn around temperature trend of ρ_c and in case of p-type poly-Si based CSJs

the doping level should be even a few times higher (not shown here).

To deepen the analysis and understanding, the pinhole density was varied in simulations between $5 \cdot 10^6 \text{ cm}^{-2}$ to $4 \cdot 10^8 \text{ cm}^{-2}$. In addition, we apply different doping densities for Phosphorus and Boron doped poly-Si layers ($N_D = 3 \cdot 10^{20} \text{ cm}^{-3}$ and $N_A = 2 \cdot 10^{19} \text{ cm}^{-3}$) as commonly observed in the literature caused by Boron's lower solubility limit in silicon and lower diffusivity of Phosphorus in silicon oxide compared to Boron [37],[38]. As we can see in Figure 5 (a) or (b) for n-type or p-type CSJ, respectively, the ρ_c is increasing with decreasing pinhole densities, which is expected since the number of pinholes influences the conductivity through the SiO_2 layer. In the case of n-type poly-Si based CSJ, the resistivity is lower compared to p-type poly-Si based CSJ, due to the higher doping level in the poly-Si layer and in the pinholes. In the case of n-type poly-Si based CSJ, we can observe a slight decrease in ρ_c with increasing temperature while for p-type poly-Si based CSJ ρ_c increases with increasing temperature. It is not favourable to increase the pinhole density to higher values than $\sim 10^8 \text{ cm}^{-2}$. Otherwise, the passivation property SiO_2 layer might not come to its full effect [21]. Hence, the poly-Si/c-Si interface

recombination inside a pinhole would prevail the passivation properties of the SiO_2 layer. Furthermore, the passivation quality of the SiO_2 layer with a higher density of pinholes would also affect its crystal structure and its passivation properties with the c-Si interface. Since these are simulations in the dark, it is not necessary to know the exact density of states and other properties at the interfaces and poly-Si layer states inside the bandgap (which heavily depend on the deposition and annealing temperature). Therefore, we have limited our further simulations to a typical pinhole density of 10^8 cm^{-2} . In this case, the high recombination velocity at poly-Si/c-Si interface inside pinhole would have a negligible impact on the current since the total current flow through the pinhole is much higher due to current crowding.

To study the effect of pinhole resistance on ρ_c we did additional simulations where the thickness of the SiO_2 layer (d_{SiO_2}) was changed in simulations and therefore the length of the pinhole resistive channel, Figure 6. Since these are 2-D simulations, the current crowding in the pinholes of the 3-D model was preserved by the described pinhole transformation. Hence the width of the 2-D pinhole is much narrower. Since the tunnelling starts to dominate the pinhole transport through SiO_2 layer for low thicknesses ($< 2 \text{ nm}$) we have simulated the ρ_c for both cases with considering tunnelling and without tunnelling, for eye guide. From Fig. 6 (b) in case of p-type poly-Si based CSJ, the ρ_c calculated without tunnelling is an almost linear function of SiO_2 thickness. This means ρ_c is purely a function of the resistivity of the pinhole channel. The contact resistance drops over an order of magnitude for thinner oxides, where comparably large tunnelling currents are possible. However, the good passivation and uniform SiO_2 films are practically achievable only for thin SiO_2 layers 1.1-1.4 nm [39],[40] therefore the simulations with thinner SiO_2 layer are only done for better understanding of main driving and limiting mechanisms. In the case of n-type CSJ, Fig. 6 (a) green curve w/o tunnelling, the ρ_c is not anymore the function of the pinhole channel resistivity, but it has a relatively large constant component. For p-type poly-Si the doping level is much lower and the related offset is negligible compared to the channel resistivity. This bias component of $\sim 0.09 \text{ m}\Omega\text{cm}^2$ is the function

Fig. 6. Simulated junction resistivity as a function of SiO_2 thickness for n-type (a) and p-type (b) poly-Si based obtained from TLM model, calculated with tunnelling (black curve with dotted symbols) and without tunnelling (green curve with cross symbols).

Fig. 7. Measured ECV profiles of n-type (solid curves) and p-type (dashed curves) poly-Si based CSJ for 30 min (red curves) and 80 min (blue curves) annealing time.

Fig. 8. All doping profiles used in simulations for n-type (a) and p-type (b) poly-Si based CSJ.

of band bending at the poly-Si/c-Si interface and also of other contact resistances, such as poly-Si and c-Si bulk resistivity and metal/poly-Si contact resistivity, that TLM method cannot efficiently distinguish [19]. Usually, the metal/poly-Si contact resistivity is much smaller than calculated ρ_c [41], the c-Si resistance is partly eliminated by the used corrected TLM method of Eidelloth et al. [19]. In the case of 30 nm thick poly-Si contact layer the area of the contact is much larger compared to the pinhole area. Therefore, the expected resistance of this poly-Si contact layer can be neglected. Thus, in this case, we will attribute this small ρ_c mostly to the band bending at the poly-Si/c-Si interface. To minimise the effect of pinhole resistance on ρ_c highly doped poly-Si layer should be used especially if the thicker SiO₂ layer with better passivation properties is required. In both cases the tunnelling is noticeable only for the SiO₂ layers below 2 nm, however, even in this case, the junction resistance is still dominated by the pinhole resistivity and band bending. Therefore, the advantage of tunnelling is seen only for the SiO₂ layer thicknesses below ~1.2 nm.

Going one step further we have analysed poly-Si based CSJs using different ECV measured doping profiles [42] with different annealing times, Fig. 7. During the annealing process,

Fig. 9. Junction resistivity for different doping profiles and one-dimensional vertical band diagram through the pinhole below the contact n-type (a) and p-type (b) CSJ.

some of the dopants diffuse from the poly-Si layer through the SiO_x layer to c-Si layer, forming a thin but highly doped region in the c-Si layer. In Fig. 7, 4 different situations are presented, the in-diffusion of donors (solid curves) and acceptors (dashed curves) in c-Si at two different annealing times. As expected, more dopants diffuse in the c-Si layer for longer annealing times. The silicon oxide interface acts as a good diffusion barrier for phosphorous atoms [43] in contrast to boron atoms which can diffuse much easier [38], hence lower acceptor doping concentration in poly-Si. Consequently higher annealing times are needed to observe similar diffusion into the c-Si layer. Thus to find out the influence of in-diffused doping profiles we have implemented a few different doping profiles into simulations (Fig. 8) according to measurements. The 30 min and 80 min annealing profiles were implemented in the following way: in poly-Si layer (including pinhole) constant doping $N_{D,A}$ was assumed, at the interface there was an abrupt change to some default value obtained from the measured ECV profiles to fit the exponential function to the measured ECV

profile in c-Si. Then the exponential fit was used until the constant doping level of c-Si was reached. The abrupt profile only assumes default values in poly-Si and c-Si layer and abrupt transition at the junction, while the default ECV profile assumes fast exponential drop (in few nanometres) from high doping level as defined by the poly-Si layer to default doping level in the c-Si layer. With these different doping profiles, we have embraced some of the most interesting theoretical situations, that could noticeably influence ρ_c .

In Fig. 9 the calculated ρ_c is shown for all four different doping profiles for n-type poly-Si based CSJ (a) with higher doping levels $N_{Dpoly} = 3 \cdot 10^{20} \text{ cm}^{-3}$ and p-type poly-Si based CSJ (b) with a lower doping level $N_{Apoly} = 2 \cdot 10^{19} \text{ cm}^{-3}$. In all cases, the default continues ECV profile with a fast drop of diffused related doping level gives the lowest ρ_c , followed by an abrupt change of doping levels. In the case of annealing approximations the 80 min annealing is preferable. For p-type CSJ the difference in annealed ECV profiles gives the smallest difference since the profiles are quite similar. This is not the case for highly doped n-type CSJ where the 80 min annealing is preferable regarding lower ρ_c . Remarkably, the abrupt change in doping between pinhole and bulk c-Si is more preferable compared to annealed ECV profiles. The reason for this can be seen from the band diagram, Figure 9, and it is related to band bending at the poly-Si/c-Si interface. Hence, larger step in the band diagram for annealed samples, in case of abrupt and default ECV profile we can see an additional very thin spike in the band profile which is the reason for the lower band step. Furthermore, in the case of highly doped poly-Si, we can see the additional bandgap narrowing is introducing different situation with higher band steps that the carriers have to overcome. Even though the default ECV doping profile shows the minimal difference compared to abrupt profile, it shows significantly lower ρ_c . The reason for that is the pinhole dimension are very small $r_p = 2 \text{ nm}$, but the poly-Si is highly doped, which allows easily to transport highly dense currents. When the crowded current hits the c-Si layer (or vice versa) it has to go through the lower doped c-Si layer with a doping level of 10^{17} cm^{-3} , with much lower free carrier concentration, which presents a higher resistive path to majority carriers. To overcome this problem, it is beneficial that the first few nanometres of the c-Si layer has higher doping (hence in-diffusion) for redistribution of the current away from the pinhole in lateral directions. This way we can swiftly decrease the volume concentration of current below the pinhole and therefore improve the CSJ ρ_c . However, increasing the in-diffusion in the c-Si layer it might potentially decrease the performance of such junction under illumination, because of the higher surface recombination velocity at CSJ [24]. This should be tested by different method since the TLM method is not suitable for this kind of study.

IV. CONCLUSION

By means of verified 2-D rigorous drift-diffusion based electrical simulations we have studied the transport mechanism of poly-Si based CSJs. The detailed analysis gave us the physical description of the happening at the CSJ, where the resistivity of the pinhole channel plays the most crucial role in the design of CSJ if the silicon oxide layer thickness is larger than 2 nm. A decrease of ρ_c can be achieved in different ways: by increasing the density of pinholes (which could reduce the passivation properties of the SiO_2 layer), lowering the SiO_2 thickness (which may also result in lower quality SiO_2) or by increasing the poly-Si doping level. Furthermore, by increasing the annealing time the in-doping in the c-Si layer would beneficially help laterally redistribute the crowded current from the pinhole to the rest of the lower doped c-Si bulk layer. The optimal values for pinholes would be doping levels around 10^{20} cm^{-3} at the densities from 10^7 cm^{-2} to 10^8 cm^{-2} . If lower doping densities of poly-Si are needed, the pinhole densities should be higher, around 10^8 cm^{-2} . In this case, it is also beneficial to keep the SiO_2 thicknesses below 3 nm preferably around 2 nm. Furthermore, the simulation shows that the inhomogeneity of the interfacial oxide thickness is not a critical part as long as the pinhole-based current flow dominates the transport mechanism.

ACKNOWLEDGEMENT

The authors thank Stefan Bordihn for a critical reading of the manuscript.

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